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10/674,951	09/30/2003	Yukio Arima	SUSU121795	5298

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EXAMINER

TRIMMINGS, JOHN P

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/674,951

Applicant(s)

ARIMA ET AL.

Examiner

John P. Trimmings

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 August 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) 1-7, 15 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 8-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

This office action is in response to the applicant's amendment dated 8/4/2006.

The applicant has cancelled claims 1-7 and 15.

The applicant has amended claims 8-14.

Claims 8-14 are pending.

Response to Amendment

1. As per Objection to the Drawings:

The applicant has not submitted a new drawing FIG. 13 as "Prior Art", therefore the examiner maintains the objection to the drawings as outlined in the previous office action dated 3/1/2006 (see below).

2. As per Objection to the Title:

In view of the new Title submitted by the applicant, the examiner withdraws the objection to the Title.

3. As per Claim Objections to the Claims:

In view of claims 1-7 and 15 being cancelled, the objections to said claims are withdrawn.

In view of the amendments to claims 8-15, the examiner withdraws the objections to claims 10-14, but maintains the objections to claims 8-9 because the amendments to said claims did not satisfy the objections (see below).

4. The indicated allowability of claim 13 is withdrawn in view of the applicant's change of scope of the claim, and in view of reference to Broseghini et al., a rejection based on the newly cited reference follows (see below).

Drawings (Repeated)

5. Figure 13 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections (Repeated)

6. Claim 8 is objected to because of the following informalities: Lines 5 and 6 of the applicant's amended claim should be corrected to recite, "... using the scan [~~the~~] scan chain ...". Appropriate correction is required.

Claim Rejections - 35 USC § 103 (New)

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7. Claims 8, 10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zyuban et al. (herein Zyuban), U.S. Patent Application Publication No. 2003/0188241, in view of Woods et al. (herein Wods), U.S. Patent Application Publication No. 2002/0162037, in view of the applicant's admitted prior art disclosure in the application pages 1-6 (herein APA), and further in view of Purdham, U.S. Patent No. 5701313.

As per claim 8:

Zyuban teaches an integrated circuit device comprising: at least one functional module (one module is chosen, see paragraphs [0002], [0003] for description of the IC functional module) which has a plurality of flip-flops (paragraph [0003]) forming a scan chain (see Abstract), performs a saving operation by outputting data in the flip-flops by a shift operation (shifting from master latch to slave latch as in the Abstract) using the scan chain (FIG. 5 60) synchronized with a saving clock signal (FIG. 5 CLOCK B), and performs a restoring operation by restoring, to the flip-flops (FIG. 5 50), the saved data (located in FIG. 5 60 latches) by a shift operation (from slave to master as in the Abstract) using the scan chain (FIG. 5 60) synchronized with a restoration clock signal (FIG. 5 CLOCK A); a power supply control unit (FIG. 5 power supply control switch 23) which selects one of the functional modules (one module is default thus selection is obvious), and controls stop and resumption of power supply (paragraph [0006]) to the selected functional module (i.e., one default module); a clock signal generator (the A, B and C clocks are generated off the chip of Zyuban) which generates a saving clock signal (FIG. 5 CLOCK B) and restoration clock signal (FIG. 5 CLOCK A) for the

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functional module (paragraph [0002], [0003]) selected by the power supply control unit (one is default); but where Zyuban fails to teach, Woods further discloses a scan controller (FIG.2 260) which, in the saving operation or restoring operation (paragraphs [0083 – 0090]), sets the functional module selected by the power supply control unit to a scan test mode (FIG.2 268), and selects the saving clock signal or restoration clock signal generated by the clock signal generator as a clock signal to be supplied for the shift operation using scan chain (clock signals A and B as in Zyuban). And in Woods, in paragraph [0012], states the advantage to be a system that saves state information without the need for an operating system. Such a system would improve Zyuban by taking advantage of internal controls during saves and restores. But where Woods fails to teach, Zyuban further teaches a shift register (the register formed by FIG. 5 60 latches) connected to the scan chain (in FIG. 5 the master 50 is connected to slave 60 forming the scan chain) wherein the shift register (FIG. 5 60) stores the save data output from the functional module (the contents of master 50) selected by the power supply control unit (default to one module) by the shift operation (from master to slave) using the scan chain synchronized with the saving clock signal (FIG. 5 CLOCK B) but fails to further disclose error correction. The APA, on page 5 and 6, discloses inherent problems within the power conservation art, where there is an increased likelihood of “soft errors” occurring during “sleep mode”. Page 6 lines 10-16 of the APA state a desirable attribute in the prior art to be the capability of minimizing the soft error problem. In the analogous art of Purdham, it is disclosed that soft errors are corrected in a transparent manner in order to minimize “soft errors” (see column 1 lines 37-50).

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Purdham discloses a memory containing an error checking and correction unit which performs error checking and correction for the save data stored in the save data storage unit when the save data is to be restored (see FIG. 5) to the functional module.

Restoring is in synchronism with a restoration clock signal (Claim 4), to the flip-flops of the functional module by the shift operation using scan chain synchronized with the restoration clock signal. Since the correction in Purdham is transparent to memory operation, it is obvious that the memory error checking and correction operations of Purdham will occur during restore clock operation (see Woods, Claim 4 and paragraphs [0082 - 0090]). One with ordinary skill in the art at the time of the invention, motivated as suggested above in Woods, the APA and Purdham, would have found it obvious to include error detection and correction (Purdham) to Zyuban in order to minimize soft error failure during sleep mode.

As per claim 10:

Purdham further discloses the device according to claim 1 or 8, wherein the error checking and correction unit comprises: an encoder which generates an error correction code from the save data (FIG.5 236), and writes the error correction code in the shift register (FIG.5 240); and a decoder (FIG.5 264) which reads out the stored save data and the corresponding error correction code (FIG.5 250) from the shift register, and decodes the save data (FIG.5 270). And in view of the motivation previously stated, the claims are rejected.

As per claim 14:

Where the prior arts of Zyuban, APA and Purdham fail, Woods further teaches the device according to claim 8, which further comprises: a compressor which compresses the save data stored in the save data storage unit (paragraph [0071]); and an expander which expands the save data compressed by the compressor when the save data is to be restored to the functional module (this is an obvious and complementary component related to the compressor herein disclosed). And in view of the motivation previously stated, the claims are rejected.

8. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zyuban et al. (herein Zyuban), U.S. Patent Application Publication No. 2003/0188241, in view of Woods et al. (herein Woods), U.S. Patent Application Publication No. 2002/0162037, in view of the applicant's admitted prior art disclosure in the application pages 1-6 (herein APA), and in view of Purdham, U.S. Patent No. 5701313 as applied to Claim 8, and further in view of Freeman et al. (herein Freeman), U.S. Patent No. 6510528. Where the references of claim 8 fail, Freeman further teaches the device, wherein the clock signal generator generates a clock signal for use in periodic error checking and correction performed in the shift register (when changing state from S1 to S0 in FIG.2 of Freeman, the scrubbing routine causes memory readout that, in accordance with Purdham, corrects any data failures). The change of state and the scrubbing routine causes the test clock generator of Woods of claim 4 to clock data out of the register as per Zyuban and into the functional module as per Zyuban FIG. 5 60 to 50. And in view of the motivation previously stated, the claims are rejected.

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zyuban et al. (herein Zyuban), U.S. Patent Application Publication No. 2003/0188241, in view of Woods et al. (herein Woods), U.S. Patent Application Publication No. 2002/0162037, in view of the applicant's admitted prior art disclosure in the application pages 1-6 (herein APA), and in view of Purdham, U.S. Patent No. 5701313 as applied to Claim 8, and further in view of Smith III, U.S. Patent No. 5502728. Where Zyuban, APA, Woods and Purdham fail, Smith III teaches the device according to claim 8, wherein the shift register stores a plurality of copies of the save data, and the error checking and correction unit performs error checking and correction by a majority operation using said plurality of copied data stored in the shift registers (FIG.5 51). And column 2 lines 36-51 state an advantage being improvement of data integrity of storage systems. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to add voter modeled data correction to the storage system of Woods and Purdham in order to improve data integrity.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zyuban et al. (herein Zyuban), U.S. Patent Application Publication No. 2003/0188241, in view of Woods et al. (herein Woods), U.S. Patent Application Publication No. 2002/0162037, in view of the applicant's admitted prior art disclosure in the application pages 1-6 (herein APA), and in view of Purdham, U.S. Patent No. 5701313 as applied to Claim 8, and further in view of Broseghini et al. (herein Broseghini), U.S. Patent No. 5761489. Where

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Zyuban, APA, Woods and Purdham fail, Broseghini teaches the device according to claim 8, wherein the shift register is storage means for a built-in self-test circuit. The feature is illustrated in FIG. 3 where shift register 94 has a dual purpose, one as a normal data register, and the other as a shift register during self-test. And in column 5 lines 30-40, such an advantage is stated, where the register is a dual-use register for internal data flow and also during scanning as a shift register. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include a dual-use register of Broseghini to the test circuit in order to save internal register space.

Conclusion

Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of


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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

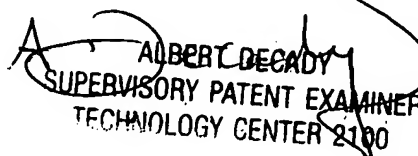
Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


John P Trimmings
Examiner
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